



TFT MODULE SPECIFICATION

## **RVT70HSMFWCA0 V1.1A**

IPS MIPI 7.0" display datasheet  
Rev. 1.1  
2026-10-07

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**Riverdi Sp. z o.o.**

Nowy Swiat 36  
80-299 Gdansk, Poland  
VAT ID: PL5842767153  
Registration number (KRS): 0000923967

**+48 587 703 116**

Office hours: 9:00 to 17:30 CET (Mon-Fri)

**[contact@riverdi.com](mailto:contact@riverdi.com)**

**[riverdi.com](https://riverdi.com)**

| ITEM                           | CONTENTS                            | UNIT              |
|--------------------------------|-------------------------------------|-------------------|
| LCD Type                       | TFT/Transmissive/Normally black/IPS | /                 |
| Size                           | 7.0                                 | Inch              |
| Viewing Direction              | Free                                | /                 |
| Outside Dimensions (W x H x D) | 181.60 x 100.60 x 8.54              | mm                |
| Active Area (W x H)            | 154.21 x 85.92                      | mm                |
| Pixel Pitch (W x H)            | 0.1506 x 0.1432                     | mm                |
| Resolution                     | 1024 (RGB) x 600                    | /                 |
| Brightness                     | 800                                 | cd/m <sup>2</sup> |
| LCD Interface Type             | MIPI                                | /                 |
| Color Depth                    | 16.7 M                              | /                 |
| Pixel Arrangement              | RGB Vertical Stripe                 | /                 |
| LCD Driver                     | EK79007AD3+EK73217BCGA              | /                 |
| With/Without Touch             | With Capacitive Touch Panel         | /                 |
| CTP IC                         | ILI2132A                            | /                 |
| LCD Input Voltage              | 3.3                                 | V                 |
| Weight                         | TBD                                 | g                 |

**Note 1.** RoHS3 compliant

**Note 2.** LCM weight tolerance: ± 5%.

## 1. REVISION RECORD

| REV NO. | REV DATE   | CONTENTS                                                        | REMARKS |
|---------|------------|-----------------------------------------------------------------|---------|
| 1.0     | 2026-07-20 | Initial release                                                 |         |
| 1.1     | 2026-10-07 | Updated drawing. For details please check revision description. |         |

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### 3. MODULE CLASSIFICATION INFORMATION

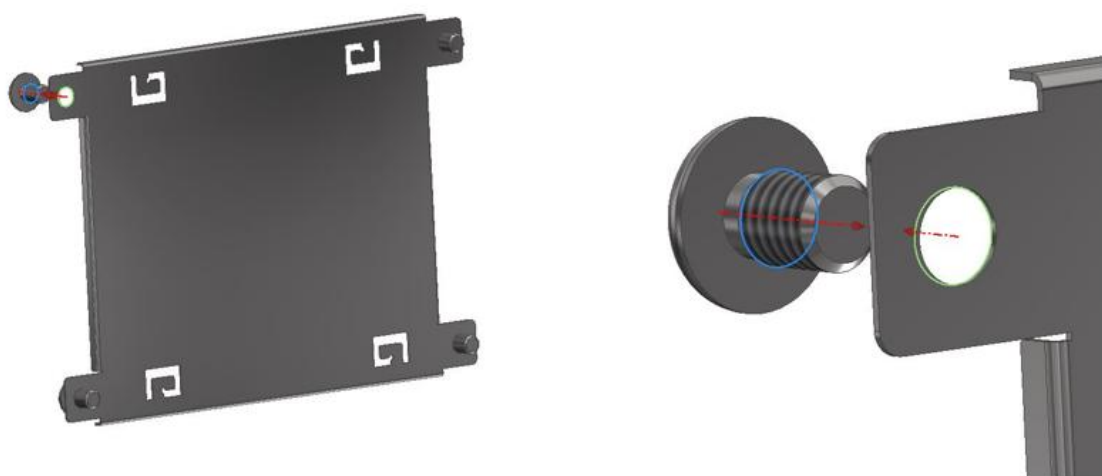
| RV | T  | 70 | H  | S  | M  | F  | W  | C  | A0  | V1.1A |
|----|----|----|----|----|----|----|----|----|-----|-------|
| 1. | 2. | 3. | 4. | 5. | 6. | 7. | 8. | 9. | 10. | 11.   |

| NO. | PARAMETER        | SYMBOL                          |
|-----|------------------|---------------------------------|
| 1.  | BRAND            | RV – Riverdi                    |
| 2.  | PRODUCT TYPE     | T – TFT Standard                |
| 3.  | DISPLAY SIZE     | 70 – 7.0”                       |
| 4.  | MODEL SERIAL NO. | H – High Brightness, IPS        |
| 5.  | RESOLUTION       | S – 1024 x 600 px               |
| 6.  | INTERFACE        | M – MIPI                        |
| 7.  | FRAME            | F – With Mounting Metal Frame   |
| 8.  | BACKLIGHT TYPE   | W – LED White                   |
| 9.  | TOUCH PANEL      | C – With Capacitive Touch Panel |
| 10. | VERSION          | A0 – aTouch                     |
| 11. | MODULE REVISION  | V1.1A                           |

## 4. ASSEMBLY

### 4.1 Mounting Frame

This product is available with mounting frame version. Thanks to the four catches attached to the side, frame provides strong assembly to the surface by mounting element (like the screw, see Figure 1). The frames are specially designed to fit Riverdi products perfectly. The diameter of the mounting hole is 3.5mm.



*Figure 1. Mounting Frame*



## 6. ABSOLUTE MAXIMUM RATINGS

| PARAMETER                 | SYMBOL   | MIN  | MAX  | UNIT | REMARK              |
|---------------------------|----------|------|------|------|---------------------|
| Analog supply voltage     | $V_{CI}$ | -0.3 | +3.6 | V    | -                   |
| Backlight forward current | $I_F$    | -    | 30   |      | For each serial LED |
| Operating Temperature     | $T_{OP}$ | -20  | 70   | °C   | -                   |
| Storage Temperature       | $T_{ST}$ | -30  | 80   | °C   | -                   |

**Note.** The above are maximum values. If exceeded, they may cause permanent damage to the unit.

## 7. ELECTRICAL CHARACTERISTICS

| PARAMETER                  | SYMBOL    | MIN     | TYP | MAX     | UNIT | REMARK                                       |
|----------------------------|-----------|---------|-----|---------|------|----------------------------------------------|
| Supply Voltage for Module  | $V_{DD}$  | 3.0     | 3.3 | 3.6     | V    | -                                            |
| Current drawn from module  | $I_{VDD}$ | 90      | 110 | 120     | mA   | -                                            |
| Logic Input Signal Voltage | $V_{IH}$  | 0.7*VDD | -   | VDD     | V    |                                              |
|                            | $V_{IL}$  | 0       | -   | 0.3*VDD | V    |                                              |
| Touch Panel Supply Current | $I_{CTP}$ | -       | 98  | -       | mA   | Measured average current, touch panel active |

## 8. TOUCH PANEL CHARACTERISTICS

| PARAMETER                            | SYMBOL                | VALUE            | REMARK                                   |
|--------------------------------------|-----------------------|------------------|------------------------------------------|
| Touch panel interface                | -                     | I <sup>2</sup> C |                                          |
| I <sup>2</sup> C 7-bit slave address | ADDR <sub>7-bit</sub> | 0x41             | Standard I <sup>2</sup> C address format |
| I <sup>2</sup> C write address       | ADDR <sub>w</sub>     | 0x82             | 8-bit address format                     |
| I <sup>2</sup> C read address        | ADDR <sub>r</sub>     | 0x83             | 8-bit address format                     |

## 9. BACKLIGHT ELECTRICAL CHARACTERISTICS

| PARAMETER                   | SYMBOL          | MIN | TYP    | MAX  | UNIT  | NOTE       |
|-----------------------------|-----------------|-----|--------|------|-------|------------|
| Backlight Driving Voltage   | V <sub>F</sub>  | 8.4 | 9.0    | 10.2 | V     | Notes 1, 2 |
| Backlight Driving Current   | I <sub>F</sub>  | -   | 270    | -    | mA    |            |
| Backlight Power Consumption | W <sub>BL</sub> | -   | 2430   | -    | mW    |            |
| Backlight Lifetime          | -               | -   | 50.000 | -    | hours | Note 3     |

**Note:** The “Operating lifetime” is defined as the module brightness decrease to 50% original brightness at Ta=25 °C and IF=270 mA. The LED lifetime could be decreased if operating IF is larger than 270 mA. Typical operating lifetime is estimated data.

## 10. ELECTRO-OPTICAL CHARACTERISTICS

| ITEM                       | SYMBOL   | CONDITION                                      | MIN   | TYP   | MAX   | UNIT              | RMK    | NOTE |
|----------------------------|----------|------------------------------------------------|-------|-------|-------|-------------------|--------|------|
| Response Time              | Tr+Tf    | $\theta=0^\circ$<br>$\phi=0^\circ$<br>Ta=25 °C | -     | 28    | 45    | ms                | FIG 2. | 4, 7 |
| Contrast Ratio             | Cr       |                                                | 600   | 800   | -     | ---               | FIG 3. | 1, 7 |
| Surface Luminance          | Lv       |                                                | -     | 800   | -     | cd/m <sup>2</sup> |        | 2, 7 |
| Uniformity                 | U        | -                                              | 70    | 75    | -     | %                 | FIG 3. | 3    |
| Viewing Angle Range        | $\theta$ | $\phi = 90^\circ$                              | 80    | 85    | -     | deg               | FIG 4. | 6    |
|                            |          | $\phi = 270^\circ$                             | 80    | 85    | -     | deg               |        |      |
|                            |          | $\phi = 0^\circ$                               | 80    | 85    | -     | deg               |        |      |
|                            |          | $\phi = 180^\circ$                             | 80    | 85    | -     | deg               |        |      |
| CIE (x, y)<br>Chromaticity | Rx       | $\theta=0^\circ$<br>$\phi=0^\circ$<br>Ta=25 °C | 0.581 | 0.611 | 0.641 | -                 | FIG 3. | 5,7  |
|                            | Ry       |                                                | 0.295 | 0.325 | 0.355 | -                 |        |      |
|                            | Gx       |                                                | 0.306 | 0.336 | 0.366 | -                 |        |      |
|                            | Gy       |                                                | 0.513 | 0.543 | 0.573 | -                 |        |      |
|                            | Bx       |                                                | 0.118 | 0.148 | 0.178 | -                 |        |      |
|                            | By       |                                                | 0.127 | 0.157 | 0.187 | -                 |        |      |
|                            | Wx       |                                                | 0.291 | 0.321 | 0.351 | -                 |        |      |
|                            | Wy       |                                                | 0.315 | 0.345 | 0.375 | -                 |        |      |
| NTSC ratio                 | -        |                                                | 40    | 47    | -     | %                 |        |      |

**Note 1.** Contrast Ratio (CR) is defined mathematically as below, for more information see Figure 2.

$$\text{Contrast Ratio} = \frac{\text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Average Surface Luminance with all black pixels (P1, P2, P3, P4, P5)}}$$

**Note 2.** Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see Figure 2.

$L_v$  = Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)

**Note 3.** The uniformity in surface luminance  $\delta$  WHITE is determined by measuring luminance at each test position 1 through 5, and then dividing the minimum luminance of 5 points luminance by maximum luminance of 5 points luminance. For more information see Figure 2.

$$\delta \text{ WHITE} = \frac{\text{Minimum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Maximum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}$$

**Note 4.** Response time is the time required for the display to transition from white to black (Rise Time,  $T_r$ ) and from black to white (Decay Time,  $T_f$ ). For additional information see Figure 1. The test equipment is BM-7A.

**Note 5.** CIE (x, y) chromaticity, the x, y value is determined by measuring luminance at each test position 1 through 5, and then make average value.

**Note 6.** For TFT module, viewing angle is the angle at which the contrast ratio is greater 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to LCD surface. For more information see Figure 3.

**Note 7.** Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80). For response time testing, the testing data is based on BM-7A. Instruments for Contrast Ratio, Surface Luminance, Luminance Uniformity, Chromaticity the test data is based on SR-3A.

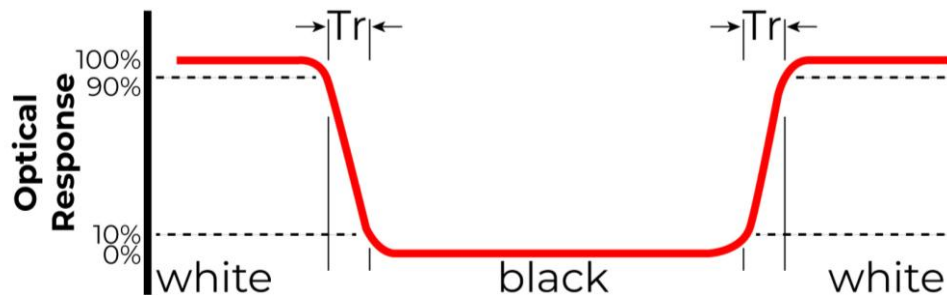


Figure 2. The definition of response time

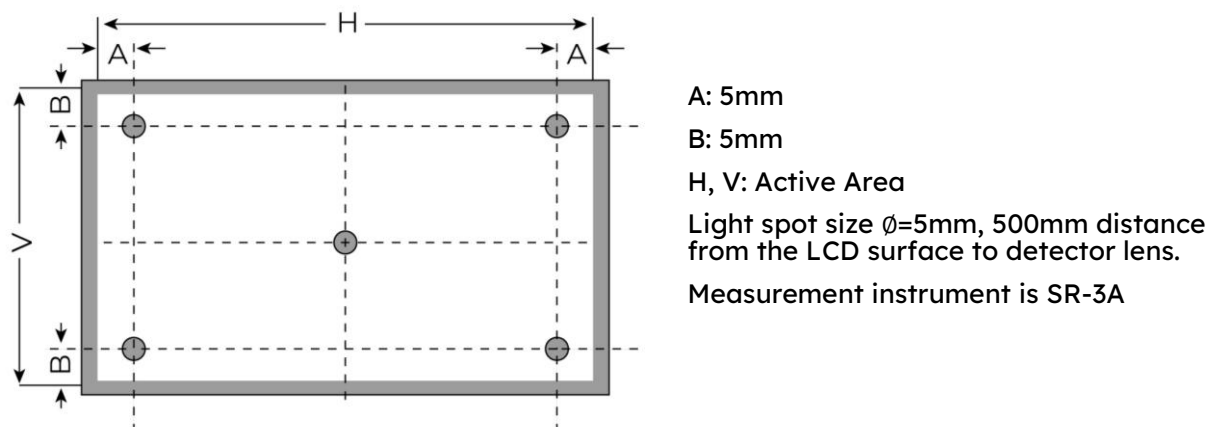


Figure 3. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE (x, y) chromaticity

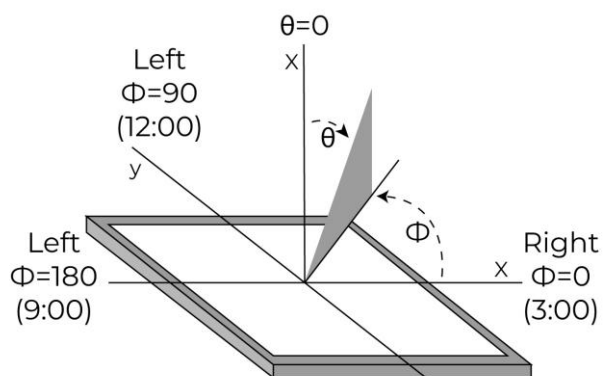


Figure 4. The definition of viewing angle

## 11. INTERFACES DESCRIPTION

### 11.1 TFT ASSIGNMENT

| PIN | SYMBOL     | I/O | DESCRIPTION                                                |
|-----|------------|-----|------------------------------------------------------------|
| 1   | NC         | -   | No connection                                              |
| 2-3 | VDD        | P   | Power for digital circuit                                  |
| 4   | NC         | -   | No connection                                              |
| 5   | RESET      | -   | Global reset pin                                           |
| 6   | STBYB      | P   | Standby mode, Normally pulled high                         |
| 7   | GND        | P   | Ground                                                     |
| 8   | MIPI_D0N   | I   | MIPI-DSI Data differential signal input pins (Data lane 0) |
| 9   | MIPI_D0P   | I   | MIPI-DSI Data differential signal input pins (Data lane 0) |
| 10  | GND        | P   | Ground                                                     |
| 11  | MIPI_D1N   | I   | MIPI-DSI Data differential signal input pins (Data lane 1) |
| 12  | MIPI_D1P   | I   | MIPI-DSI Data differential signal input pins (Data lane 1) |
| 13  | GND        | P   | Ground                                                     |
| 14  | MIPI_D2N   | I   | MIPI-DSI Data differential signal input pins (Data lane 2) |
| 15  | MIPI_D2P   | I   | MIPI-DSI Data differential signal input pins (Data lane 2) |
| 16  | GND        | P   | Ground                                                     |
| 17  | MIPI_DCLKN | I   | MIPI-DSI CLOCK differential signal input pins              |
| 18  | MIPI_DCLKP | I   | MIPI-DSI CLOCK differential signal input pins              |
| 19  | GND        | P   | Ground                                                     |
| 20  | MIPI_D3N   | I   | MIPI-DSI Data differential signal input pins (Data lane 3) |
| 21  | MIPI_D3P   | I   | MIPI-DSI Data differential signal input pins (Data lane 3) |
| 22  | GND        | P   | Ground                                                     |

|              |      |   |                      |
|--------------|------|---|----------------------|
| <b>23-24</b> | NC   | - | No connection        |
| <b>25</b>    | GND  | P | Ground               |
| <b>26-29</b> | NC   | - | No connection        |
| <b>30</b>    | GND  | P | Ground               |
| <b>31-32</b> | LED- | P | LED Cathode          |
| <b>33</b>    | L/R  | I | Horizontal Inversion |
| <b>34</b>    | U/D  | I | Vertical Inversion   |
| <b>35-38</b> | NC   | - | No connection        |
| <b>39-40</b> | LED+ | P | LED Anode            |

**Note.** U/D R/L Function description

| SETTING OF SCAN CONTROL INPUT |      | SCANNING DIRECTION        |
|-------------------------------|------|---------------------------|
| U/D                           | L/R  |                           |
| GND                           | DVDD | Up to down, left to right |
| DVDD                          | GND  | Down to up, right to left |
| GND                           | GND  | Up to down, right to left |
| DVDD                          | DVDD | Down to up, left to right |

## 11.2 Touch Panel Connector

| PIN      | SYMBOL  | DESCRIPTION             |
|----------|---------|-------------------------|
| <b>1</b> | USB_GND | USB Ground              |
| <b>2</b> | USB_VDD | USB Power for CTP, 5.0V |
| <b>3</b> | USB_D-  | USB Data signal-        |
| <b>4</b> | USB_D+  | USB Data signal+        |
| <b>5</b> | I2C_GND | I2C Ground              |

|           |         |                                           |
|-----------|---------|-------------------------------------------|
| <b>6</b>  | I2C_VDD | I2C Power for CTP 3.3V                    |
| <b>7</b>  | I2C_RST | I2C Reset pin, active low                 |
| <b>8</b>  | I2C_SCL | I2C Clock input                           |
| <b>9</b>  | I2C_INT | I2C Interrupt signal from CTP, active low |
| <b>10</b> | I2C_SDA | I2C Data signal                           |

### 11.3 CN1 assignment

| PIN      | SYMBOL  | DESCRIPTION                |
|----------|---------|----------------------------|
| <b>1</b> | USB_VDD | USB_Power for CTP, DC 5.0V |
| <b>2</b> | USB_D-  | USB_Data signal -          |
| <b>3</b> | USB_D+  | USB_Data signal +          |
| <b>4</b> | USB_GND | USB_Ground                 |

## 12. TIMING CHART

### 12.1 Timing Characteristic

#### 12.1.1 DE Mode

| PARAMETER                       | SYMBOL   | MIN  | TYP  | MAX  | UNIT |
|---------------------------------|----------|------|------|------|------|
| DCLK frequency @Frame rate=60HZ | fclk     | 40.8 | 51.2 | 67.2 | MHz  |
| Horizontal display area         | Thd      | 1024 |      |      | DCLK |
| HSYNC period time               | Th       | 1114 | 1344 | 1400 | DCLK |
| HSYNC blanking                  | Thb+thfp | 90   | 320  | 376  | DCLK |
| Vertical display area           | Tvd      | 600  |      |      | H    |
| VSYNC period time               | Tv       | 610  | 635  | 800  | H    |
| VSYNC blanking                  | Tvb+tvfp | 10   | 35   | 200  | H    |

#### 12.1.2 HV Mode (Horizontal input timing)

| PARAMETER                       | SYMBOL | MIN  | TYP  | MAX  | UNIT |
|---------------------------------|--------|------|------|------|------|
| DCLK frequency @Frame rate=60Hz | Fclk   | 44.9 | 51.2 | 63   | MHz  |
| Horizontal display area         | Thd    | 1024 |      |      | DCLK |
| 1 Horizontal line               | Th     | 1200 | 1344 | 1400 | DCLK |
| HSYNC Pulse Width               | Thpw   | 1    | -    | 140  | DCLK |
| HSYNC back porch                | Thbp   | 160  | 160  | 160  | DCLK |
| HSYNC front porch               | Thfp   | 16   | 160  | 216  | DCLK |

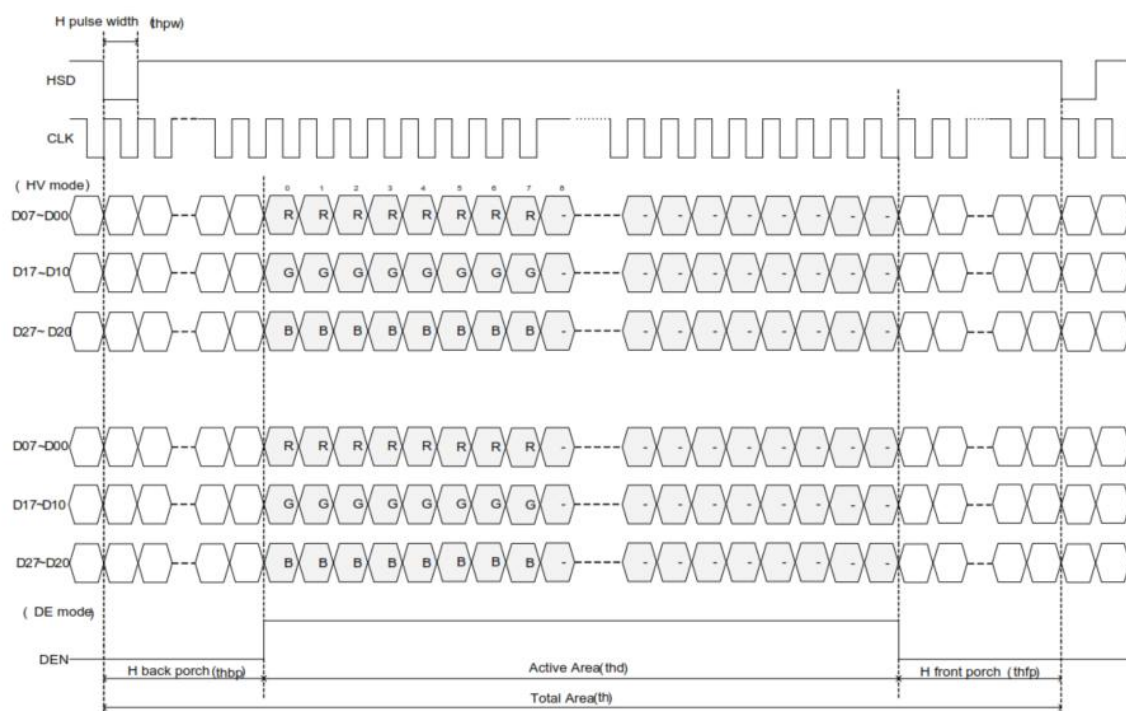
#### 12.1.3 HV Mode (Vertical input timing)

| PARAMETER             | SYMBOL | MIN | TYP | MAX | UNIT |
|-----------------------|--------|-----|-----|-----|------|
| Vertical display area | Tvd    | 600 |     |     | H    |
| 1 VSYNC period time   | Tv     | 624 | 635 | 750 | H    |

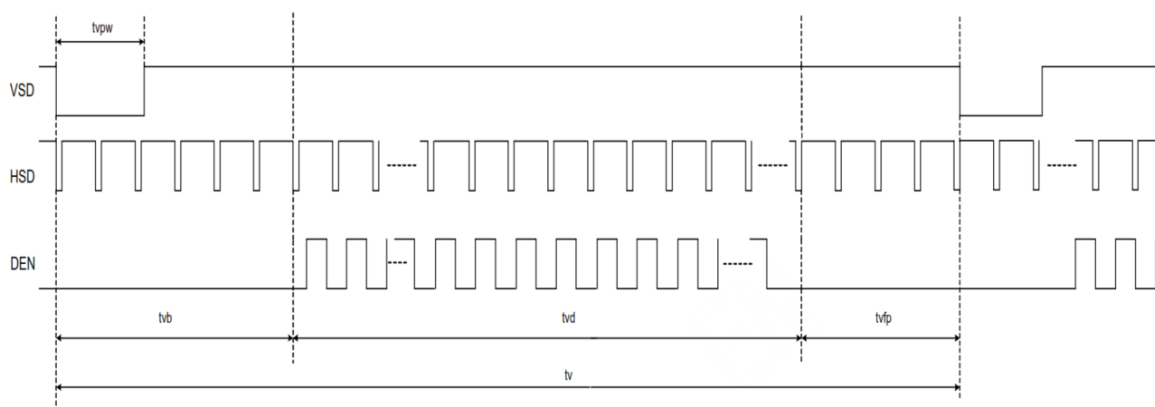
|                   |      |    |    |     |   |
|-------------------|------|----|----|-----|---|
| VSYNC Pulse Width | Tvpw | 1  | -  | 20  | H |
| VSYNC back porch  | Tvbp | 23 | 23 | 23  | H |
| VSYNC front porch | Tvfp | 1  | 12 | 127 | H |

## 12.2 Input timing diagram

### Horizontal input timing



### Vertical input timing

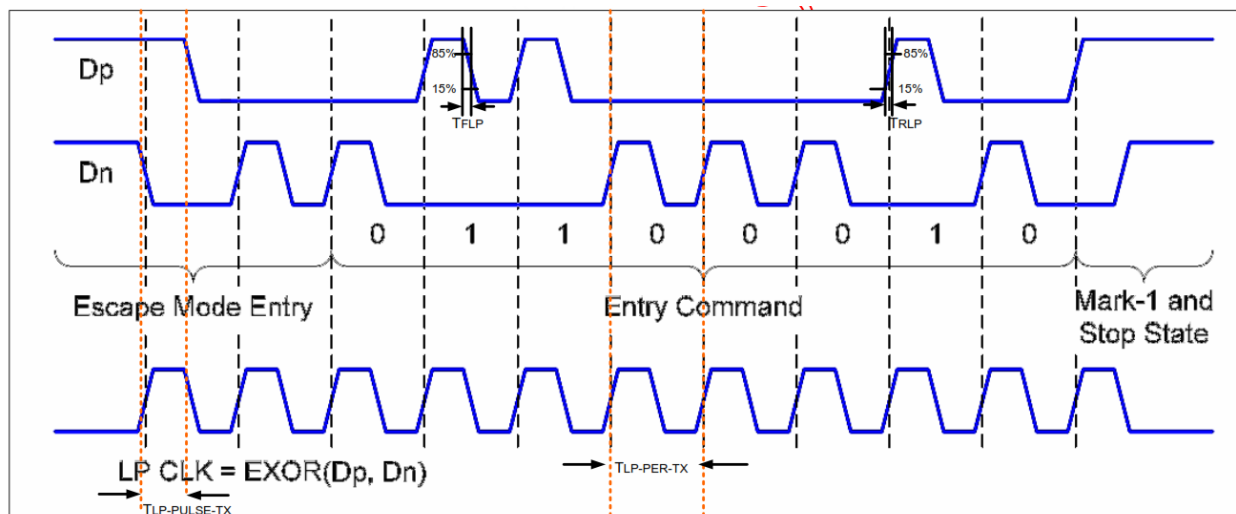


## 12.3 MIPI-DSI timings

The MIPI display we are using is together with THS\_ZERO time. Unfortunately, Driver MIPI does not meet the minimum value allowed by the MIPI standard. If the THS\_ZERO time is in the lower range, the Driver may not initialize correctly. This results in “jumping” of the image. For correct operation of the display, it is necessary to modify the THS\_ZERO parameter in the DSI-PHY controller. The default value of THS\_ZERO should be changed to a value of about 213 ns.

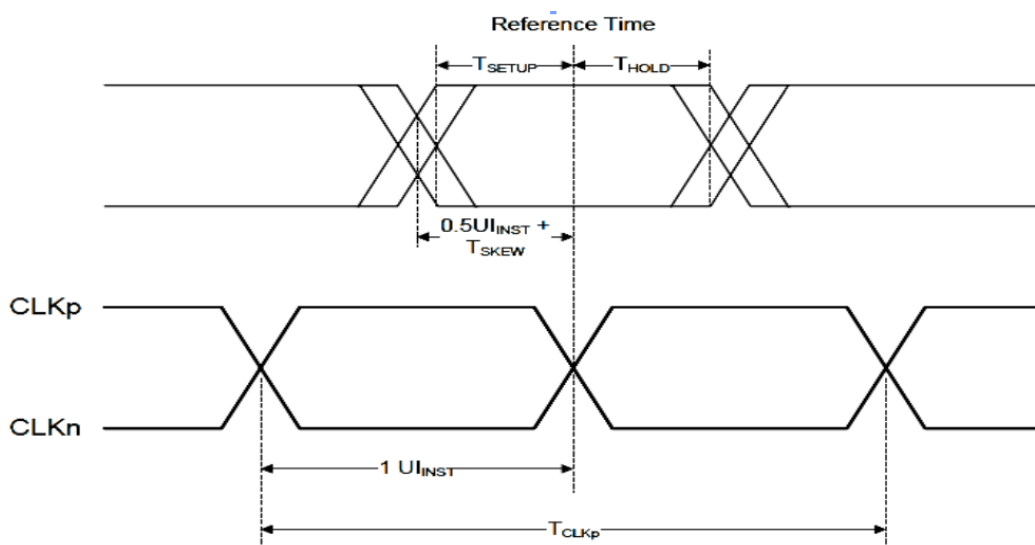
## 12.4 Low power transmitter AC characteristic

| PARAMETER                              |                                                                            | SYMBOL                             | MIN | TYP | MAX | UNIT |
|----------------------------------------|----------------------------------------------------------------------------|------------------------------------|-----|-----|-----|------|
| 15%~85% rising time and falling time   |                                                                            | T <sub>RLP</sub> /T <sub>FLP</sub> | -   | -   | 25  | ns   |
| 30%~85% rising time and falling time   |                                                                            | T <sub>REOT</sub>                  | -   | -   | 35  |      |
| Pulse width of LP exclusive - OR clock | First LP EXOR clock pulse after STOP state or LAST pulse before stop state | T <sub>LP-PULSE-TX</sub>           | 40  | -   | -   |      |
|                                        | All other pulses                                                           |                                    | 20  | -   | -   |      |
| Period of the LP EXOR clock            |                                                                            | T <sub>LP-PER-TX</sub>             | 90  | -   | -   |      |
| Slew Rate @CLOAD =0pF                  |                                                                            | δV /δt <sub>SR</sub>               | 30  | -   | 500 |      |
| Slew Rate @CLOAD =5pF                  |                                                                            |                                    | 30  | -   | 200 |      |
| Slew Rate @CLOAD =20pF                 |                                                                            |                                    | 30  | -   | 150 |      |
| Slew Rate @CLOAD =70pF                 |                                                                            |                                    | 30  | -   | 100 |      |
| Load Capacitance                       |                                                                            | T <sub>RLP</sub>                   | -   | -   | 70  | pF   |



## 12.5 High speed transmission

| PARAMETER                                          | SYMBOL          | MIN   | TYP | MAX  | UNIT        |
|----------------------------------------------------|-----------------|-------|-----|------|-------------|
| UI instantaneous                                   | $UI_{INST}$     | 2     | -   | 12.5 | ns          |
| Data to Clock Skew (measured at transmitter)       | $T_{SKEW(TX)}$  | -0.15 | -   | 0.15 | $UI_{INST}$ |
| Data to Clock Setup time<br>(Measured at receiver) | $T_{SETUP(RX)}$ | 0.15  | -   | -    |             |
| Data to Clock Hold time<br>(Measured at receiver)  | $T_{HOLD(RX)}$  | 0.15  | -   | -    |             |
| 20%~80% rising time and falling time               | $T_R, T_F$      | 150   | -   | -    | ps          |



## 12.6 High speed clock transmission

| PARAMETER                                                                                                                 | SYMBOL                            | MIN        | TYP | MAX | UNIT |
|---------------------------------------------------------------------------------------------------------------------------|-----------------------------------|------------|-----|-----|------|
| Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode | $T_{\text{CLK-POST}}$             | $60+52U_I$ | -   | -   | ns   |
| Detection time that the clock has stopped toggling                                                                        | $T_{\text{CLK-MISS}}$             | -          | -   | 60  |      |
| Time to drive LP-00 to prepare for HS clock transmission                                                                  | $T_{\text{CLK-PREPARE}}$          | 38         | -   | 95  |      |
| Minimum lead HS-0 drive period before starting clock                                                                      | $T_{\text{CLK-PREPARE+CLK-ZERO}}$ | 300        | -   | -   |      |
| Time to enable Clock Lane receiver line termination measured from when Dn cross $V_{\text{IL,MAX}}$                       | $T_{\text{HS-TERM-EN}}$           | -          | -   | 38  | UI   |
| Minimum time that the HS clock must be prior to any associated data lane beginning the transmission from LP to HS mode    | $T_{\text{CLK-PRE}}$              | 8          | -   | -   |      |

Time to drive HS differential state after last payload clock bit of a HS transmission burst

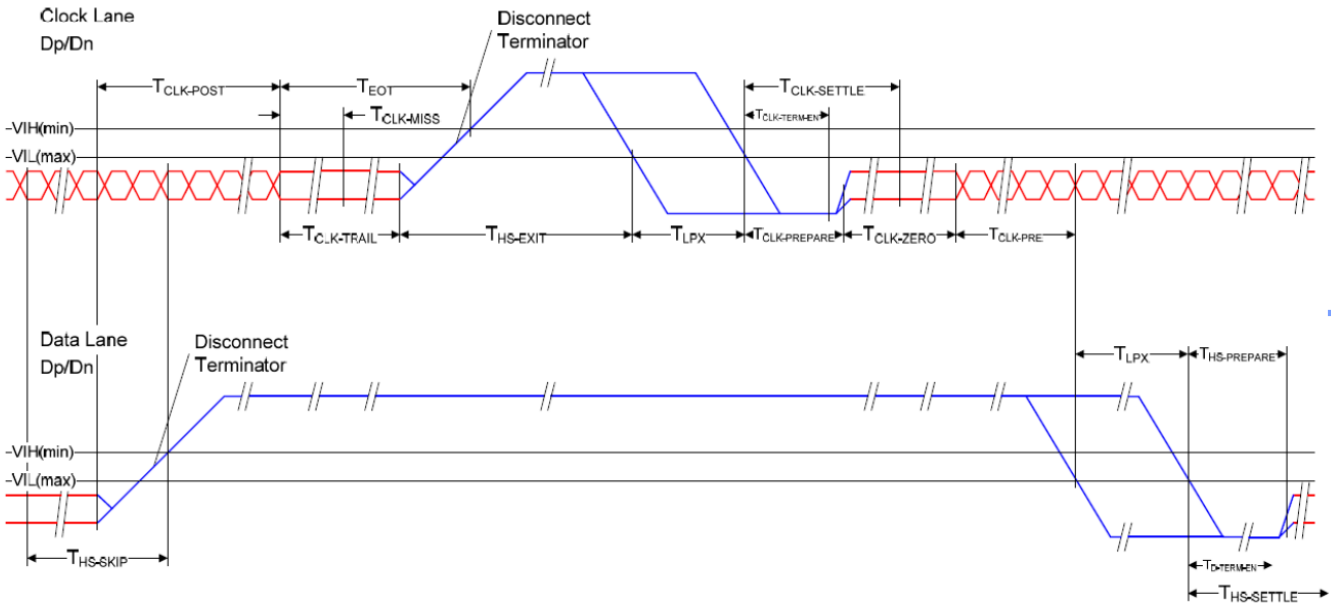
 $T_{\text{CLK-TRAIL}}$ 

60

-

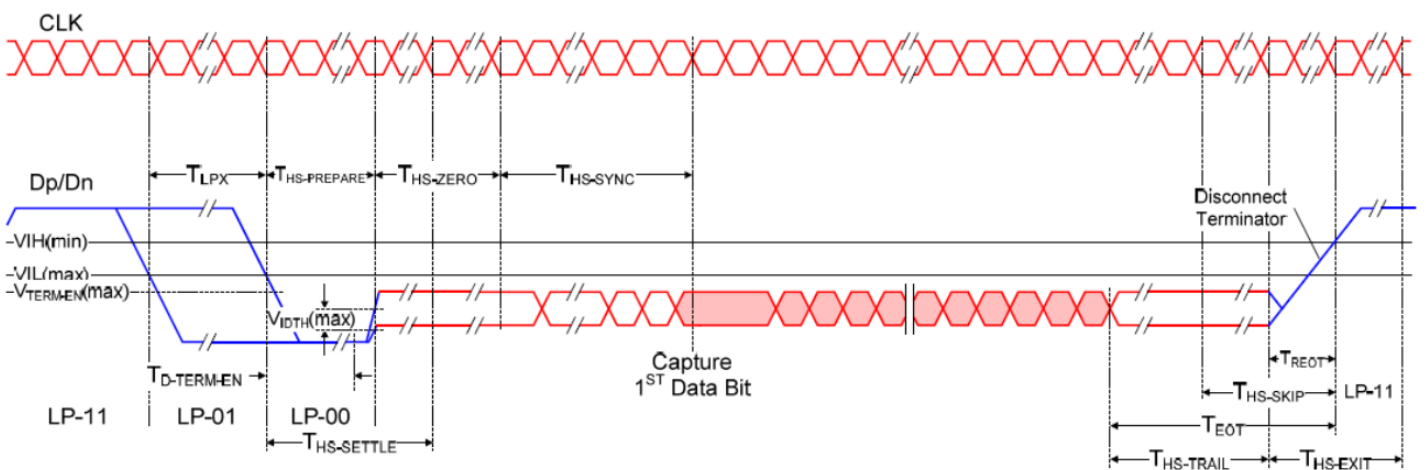
-

ns



The diagram illustrates the timing of a high-speed (HS) transmission burst. It shows two signals: Clock Lane Dp/Dn (red) and Data Lane Dp/Dn (blue). The Clock Lane signal transitions from a high state to a low state, then back to high. The Data Lane signal transitions from a high state to a low state, then back to high. Key timing parameters are labeled:  $T_{\text{CLK-POST}}$ ,  $T_{\text{EOT}}$ ,  $T_{\text{CLK-MISS}}$ ,  $T_{\text{CLK-SETTLE}}$ ,  $T_{\text{CLK-TERMEN}}$ ,  $T_{\text{CLK-TRAIL}}$ ,  $T_{\text{HS-EXIT}}$ ,  $T_{\text{LPX}}$ ,  $T_{\text{CLK-PREPARE}}$ ,  $T_{\text{CLK-ZERO}}$ ,  $T_{\text{CLK-PRE}}$ ,  $T_{\text{HS-SKIP}}$ ,  $T_{\text{HS-PREPARE}}$ ,  $T_{\text{D-TERMEN}}$ ,  $T_{\text{HS-SETTLE}}$ , and  $T_{\text{HS-TRAIL}}$ . The diagram also shows the Disconnect Terminator and the HS differential state transitions.

## 12.7 High speed data transmission in bursts



The diagram illustrates the timing of high-speed (HS) data transmission in bursts. It shows three signals: CLK (red), Dp/Dn (blue), and LP (green). The CLK signal is a periodic square wave. The Dp/Dn signal transitions from a high state to a low state, then back to high. The LP signal transitions from a high state to a low state, then back to high. Key timing parameters are labeled:  $T_{\text{LPX}}$ ,  $T_{\text{HS-PREPARE}}$ ,  $T_{\text{HS-ZERO}}$ ,  $T_{\text{HS-SYNC}}$ ,  $T_{\text{D-TERMEN}}$ ,  $T_{\text{HS-SETTLE}}$ ,  $T_{\text{EOT}}$ ,  $T_{\text{HS-SKIP}}$ ,  $T_{\text{HS-TRAIL}}$ ,  $T_{\text{HS-EXIT}}$ , and  $T_{\text{HS-TRAIL}}$ . The diagram also shows the Disconnect Terminator and the HS differential state transitions.

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## 13. INITIALIZATION CODE

```
DCS_Short_Write_NP(0x01); //Software Reset
Delay (120);
Generic_Short_Write_1P(0xB2,0x70); //Set Channels  2LANE:0x50; 3LANE:0x60; 4LANE:0x70
Generic_Short_Write_1P(0x80,0x4B); //Set Gamma voltage
Generic_Short_Write_1P(0x81,0xFF); //Set Gamma voltage
Generic_Short_Write_1P(0x82,0x1A); //Set Gamma voltage
Generic_Short_Write_1P(0x83,0x88); //Set Gamma voltage
Generic_Short_Write_1P(0x84,0x8F); //Set Gamma voltage
Generic_Short_Write_1P(0x85,0x35); //Set Gamma voltage
Generic_Short_Write_1P(0x86,0xB0); //Set Gamma voltage
DCS_Short_Write_NP(0x11); //Exit Sleep Mode
Delay (120);
DCS_Short_Write_NP(0x29); //Display on; 0x28 is display off
Delay (20);
```

## 14. INSPECTION

Standard acceptance/rejection criteria for TFT module according to document available [here](#).

## 15. RELIABILITY TEST

| NO. | TEST ITEM                           | TEST CONDITION                                                                                                                                 | NOTE      |
|-----|-------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| 1   | High Temperature Storage            | 80°C/120 hours                                                                                                                                 | A,B,C,D,E |
| 2   | Low Temperature Storage             | -30°C/120 hours                                                                                                                                |           |
| 3   | High Temperature Operating          | 70 °C /120 hours                                                                                                                               |           |
| 4   | Low Temperature Operating           | -20°C/120 hours                                                                                                                                |           |
| 5   | High Temperature and High Humidity  | +60°C, 90%RH, 120hrs                                                                                                                           |           |
| 6   | Thermal Cycling Test (No operation) | -20°C /30 min ~ +70°C /30 min for a total 10 cycles, Start with cold temperature and end with high temperature.                                | A,B,C,D,E |
| 7   | Vibration Test                      | Sweep:10Hz~55Hz~10Hz 2G<br>2 hours for each direction of X. Y. Z.<br>(6 hours for total)                                                       | A,B,C,D,E |
| 8   | Package Vibration Test              | Random Vibration :<br>0.015G*G/Hz from 5-200HZ,<br>-6dB/Octave from 200-500HZ<br>2 hours for each direction of X. Y. Z.<br>(6 hours for total) | A,B,C,D,E |
| 9   | Package Drop Test                   | Height: 60 cm<br>1 corner, 3 edges, 6 surfaces                                                                                                 | A,B,C,D,E |
| 10  | ESD                                 | Contact=+/-4KV, Air=+/-8KV,(R=330R,C=150pF), 1 sec,9point,10times/point;                                                                       | A,B,C,D,E |

### Notes

- A. LCM each function is OK.
- B. LCM appearance inspection without abnormalities (Including scratch, damage, corrosion and serious deformation)
- C. LCM brightness above the Min. value of Spec.
- D. Luminance uniformity above the Min. value of Spec.
- E. Color chromaticity within tolerance range.

## 16. LEGAL INFORMATION

CE marking is usually obligatory only for a complete end product. Riverdi display modules are semi-finished goods which are used as inputs to become part of the finished products.

Therefore, Riverdi display modules are not CE marked.

This is not a standalone product. It was designed as an electronic component. It needs integration with a whole system to be fully functional.

Riverdi grants the guarantee for the proper operation of the goods for a period of 12 months from the date of possession of the goods. If in a consequence of this guaranteed execution the customer has received the defects-free item as replacement for the defective item, the effectiveness period of this guarantee shall start anew from the moment the customer receives the defects-free item.

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## 17. CONTACT

### Your Success is Our Priority

Stuck on a technical challenge? Need expert guidance?  
Our dedicated support team is just a message away.

Contact us at

[\*\*contact@riverdi.com\*\*](mailto:contact@riverdi.com)

We're here to ensure your project's success, every step of the way!